UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/786,643	02/25/2004	Kuan-Lun Cheng	TSM03-0698	3090

43859 7590 10/25/2004

SLATER & MATSIL, L.L.P.
17950 PRESTON ROAD, SUITE 1000
DALLAS, TX 75252

EXAMINER	
QUINTO, KEVIN V	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 10/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/786,643	CHENG ET AL.	
	Examiner	Art Unit	
	Kevin Quinto	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *15 March 2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-32 are rejected under 35 U.S.C. 102(e) as being anticipated by Shimizu et al. (United States Patent Application No. US 2004/0029323 A1).

4. In reference to claims 1 and 14, Shimizu et al. (United States Patent Application No. US 2004/0029323 A1, hereinafter referred to as the "Shimizu" reference) discloses a similar device and method. Figures 5(a)-5(c) illustrate a fabrication method for a CMOS structure having a silicon nitride layer (16) in which the stress is relaxed by implantation by ions. Shimizu discloses that any ions are usable (p.8, paragraph 111).

5. With regard to claims 2, 3, 5, 7, 15, 16, 18, 19, 20, 22, 23, and 24, figures 5(a)-5(c) illustrates the use of a photoresist mask in order to prevent ion implantation in all but the selected area. Shimizu also discusses the use of the photoresist mask to block the NMOS or the PMOS area of the structure (p.7, paragraph 106 and p.8, paragraph 111).

6. In reference to claims 4, 6, 17, and 21, Shimizu makes it clear that the stress to be modified may be compressive or tensile (p.8, paragraph 108 and p.8, paragraph 111).

7. In reference to claim 8, Shimizu (US 2004/0029323 A1) discloses a similar device. Figures 5(a)-5(c) illustrate a CMOS structure with a silicon nitride layer (16) which overlies one or more NMOS structures and one or more PMOS structures. Shimizu does not disclose the use of the silicon nitride as a contact etch stop layer. However a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963). Therefore the limitation describing the silicon nitride layer as the contact etch stop layer is not patentably distinguishable over the Shimizu reference. First areas of the nitride layer (16) overlying one type of device are implanted by ions

while second areas of the layer (16) are not implanted by ions. Shimizu discloses that any ions are usable (p.8, paragraph 111).

8. In reference to claims 9 and 12, Shimizu discloses that the silicon nitride layer (16) is formed by plasma enhanced chemical vapor deposition (p.7, paragraph 105).

9. With regard to claim 10, Shimizu makes it clear that the silicon nitride layer may be formed by a thermal CVD process (p.2, paragraphs 23-24).

10. With regard to claims 11 and 13, figures 5(a)-5(c) illustrates the use of a photoresist mask in order to prevent ion implantation in all but the selected area. Shimizu also discusses the use of the photoresist mask to block the NMOS or the PMOS area of the structure (p.7, paragraph 106 and p.8, paragraph 111).

11. In reference to claim 25, Shimizu (US 2004/0029323 A1) discloses a similar method. Figures 5(a)-5(c) illustrate a process for fabricating a CMOS structure with a silicon nitride layer (16) which overlies one or more NMOS structures and one or more PMOS structures. Shimizu does not disclose the use of the silicon nitride as a contact etch stop layer. However a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963). Therefore the limitation describing

the silicon nitride layer as the contact etch stop layer is not patentably distinguishable over the Shimizu reference. Areas of the nitride layer (16) overlying one type of device are implanted by ions while other areas of the layer (16) are simultaneously prevented from being implanted with ions. Shimizu discloses that any ions are usable (p.8, paragraph 111).

12. With regard to claims 26, 27, 30, 32, figures 5(a)-5(c) illustrates the use of a photoresist mask in order to prevent ion implantation in all but the selected area. Shimizu also discusses the use of the photoresist mask to block the NMOS or the PMOS area of the structure (p.7, paragraph 106 and p.8, paragraph 111).

13. In reference to claims 28 and 31, Shimizu discloses that the silicon nitride layer (16) is formed by plasma enhanced chemical vapor deposition (p.7, paragraph 105).

14. With regard to claim 29, Shimizu makes it clear that the silicon nitride layer may be formed by a thermal CVD process (p.2, paragraphs 23-24).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (571) 272-1920. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The

fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KVQ

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800